4-port digital isolator based on on-chip transformer

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Abstract: The design and fabrication results of a 4-port digital isolator based on an on-chip transformer for galvanic isolation are presented. An ON–OFF keying modulation scheme is used to transmit the digital signal. The proposed digital isolator is fabricated by the 0.18 μm CMOS process. A test chip can achieve a 1 MHz signal bandwidth, a 40 ns propagation delay, a 35.5 mW input power and a 50 mA drive output current. The proposed digital isolator is pin-compatible, of small volume and low power replacement for the common 4-port optocoupler.

Key words: optocoupler; 4-port; digital isolator; on-chip transformer
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1. Introduction

Galvanic isolation is needed to protect systems and end users from potentially hazardous voltages in many applications including industrial control, military and space applications, medical electronics, and many others[1, 2]. Galvanic isolation can be achieved in multiple ways. Traditionally, optocouplers have been dominating the isolation market for their high isolation capability and relatively low cost. However, optocouplers have some intrinsic problems, such as low speed (1–50 Mbps), high power dissipation, degradation of the LED, and low common-mode transient immunity (CMTI). In addition, the performance of optocouplers is weakened by the changing of their current transfer ratio (CTR) with operating conditions and temperature.

Digital isolators fabricated in complementary metallic oxide semiconductor (CMOS) process technology are gaining favor from designers because of their significant advantages in terms of speed (100–150 Mbps), power dissipation, propagation delays, and more[3, 4]. Digital isolators using magnetic coupling[5–7], capacitive coupling[8, 9] and giant magneto resistive (GMR)[10] methods have been reported in the academic literature and commercially. They are challenging the optocouplers. However, the current digital isolators which usually provide six ports are not package- and pin-compatible to the common 4-port optocouplers. It can be difficult to replace optocouplers directly in some old designs.

In this paper, a 4-port digital isolator based on an on-chip transformer is proposed to supersede the 4-port optocoupler directly. The design can increase the signal bandwidth to 1 MHz and reduce the system volume and cost. The proposed digital isolator is suitable for the replacement of the common 4-port optocoupler, and it has higher signal bandwidth and lifetime. This paper is organized as follows. Section 2 describes the circuit schematic and design principles. Section 3 presents the simulation and measurement results, and finally conclusions are presented in Section 4.

2. System design

Fig. 1 shows the block diagram of the proposed digital isolator. The system consists of a cross-coupled oscillator, an on-chip transformer, a demodulation module, and an open drain (OD) gate circuit. It provides four ports including INPUT, GND1, OUTPUT, and GND2, which is pin-compatible to the common 4-port optocoupler. The proposed digital isolator uses an ON–OFF keying (OOK) modulation scheme to transmit the digital logic signal. The oscillator sends a carrier signal across the transformer to represent one digital state, and sends no signal to represent the other digital state. The demodulation module demodulates the received signal. The OD gate circuit provides the drive current as the output.

Fig. 2 shows the circuit schematic. When V_{in} is greater than the threshold voltage of NMOS transistors, the carrier signal is generated by alternately turning on MN1 and MN2, and transmitted to the secondary side of the transformer. The received signal is demodulated by the full-wave bridge rectifier, and then OD gate circuit MN5 is charged until it is turned on. The output is connected to ground and V_{out} is set to low. When V_{in} is lower than the threshold voltage of NMOS transistors, the oscillator has no carrier signal by turning off the MN1 and MN2. The OD gate circuit is off. The output is connected to the supply voltage through the pull-up resistor R_{UP}, and V_{out} is set to high.

2.1. On-chip transformer

It can be seen from the well known equation $f = 1/(2\pi\sqrt{LC})$ that L and C determine the oscillation frequency. Here, L is the equivalent inductance of the transformer, which is directly determined by the area of the transformer. C is the parasitic gate capacitance of the cross-coupled NMOS transistor. In order to satisfy the desired oscillation frequency, the on-chip transformer has been designed. In the case that the transformer area is limited to 500 μm^2, the coil with more turns can gain greater inductance to reduce the

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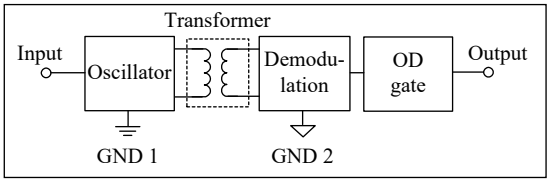

Fig. 1. Block diagram of the proposed digital isolator.

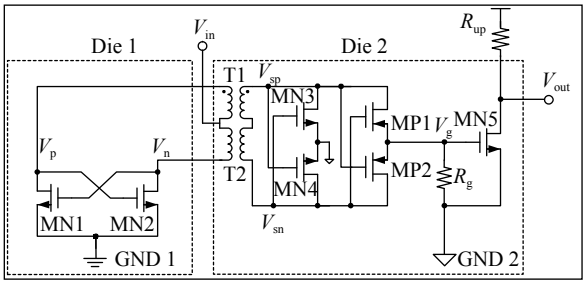

Fig. 2. Circuit schematic of the proposed digital isolator.

Table 1. The geometric parameters of transformer.

Parameter	D_{out} (μm)	w (μm)	s (μm)	t (μm)	N
Primary	500	5	0.6	0.87	32
Secondary	500	5	0.4	0.525	34

switching loss. The on-chip stacked spirals transformer with its center tape connected to V_{in} is designed by the 3D finite element modeling (FEM) tool. The geometric parameters of the primary and secondary coil of the transformer include outer diameter (D_{out}), trace width (w), trace separation (s), thickness (t), and turns (N), as shown in Table 1. At 320 MHz, the simulated inductance and quality factor for primary and secondary coils are 216 nH, 262 nH, 2.1, and 1.1, respectively.

The on-chip transformer is implemented in a 0.18 μm CMOS process and the cross-section is shown in Fig. 3. A patterned ground shield (PGS) is used to improve the performance of the transformer. A 2.125 μm thick silicon dioxide and silicon nitride mixture is used as the insulating layer, which is tested to provide 0.4 kV isolation voltage.

2.2. Cross-coupled oscillator

The schematic of the cross-coupled oscillator studied in this paper is shown in Fig. 4. Two CMOS transistors MN1 and MN2 implemented in a cross-coupled configuration together with transformer form the sustaining oscillation. L_1 and L_2 are the two primary inductors of the transformer.

The start-oscillating condition of the cross-coupled oscillator can be achieved by:

$$\frac{g_m}{2} \geqslant \frac{1}{R} \times \alpha, \tag{1}$$

where g_m is the transconductance, R is the equivalent resistance of the primary coil, and $\alpha = 2$–3 is the safety factor. The driving current provided by the CMOS transistor can be calculated by the Shichman-Hodge equation as follows:

$$I_D = k\left(V_{gs} - V_{th}\right)V_{ds} + \frac{kV_{ds}^2}{2}, \tag{2}$$

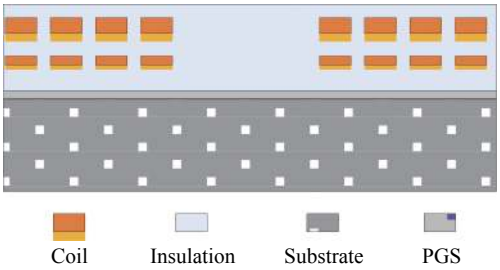

Fig. 3. (Color online) Cross-sectional of transformer.

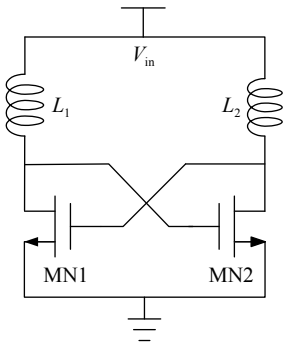

Fig. 4. Cross-coupled oscillator.

where k is transistor gain, V_{gs} is gate-source voltage, V_{ds} is drain-source voltage, and V_{th} is threshold voltage. At a 10 mA dynamic current, the width-to-length ratio of MN1 and MN2 are calculated as 100 μm/1.5 μm, and g_m is calculated as 0.0998 s.

According to Ref. [11], it is assumed that only the first and the second harmonic of the output voltage are considered, the amplitude of the first harmonic is five times larger than the second harmonic, and thus the differential outputs of oscillator V and oscillation frequency f are given by:

$$V = 2h_1 + 2h_1/5, \tag{3}$$

$$f = \frac{1}{T_n} = \frac{1}{\sqrt{LC}\left\{2\pi + 4\sin^{-1}\left[(V_{DD} - K_0)/K_1\right]\right\}}, \tag{4}$$

$$K_0 = \frac{\xi}{\sqrt{W}} \frac{\sqrt[4]{C}}{\sqrt[4]{L}}, \tag{5}$$

where h_1 is the first harmonic amplitude. L is the equivalent inductance of the primary coil of the transformer. C is the parasitic gate capacitance of the cross-coupled NMOS transistor. V_{DD} is the supply voltage. K_1 is approximated by the first harmonic amplitude. $\xi = 0.052$ is a constant coefficient. W is the transistor width. The oscillation amplitude and oscillation frequency of the cross-coupled oscillator designed in this paper are calculated as 14.3 V and 327.3 MHz.

2.3. Demodulation module

The demodulation module consists of rectifying circuit, discharge resistance R_g, and OD gate circuit. Both NMOS pairs and PMOS pairs are used as a rectifier. MN5 is an OD gate circuit which provides output drive current. The prin-

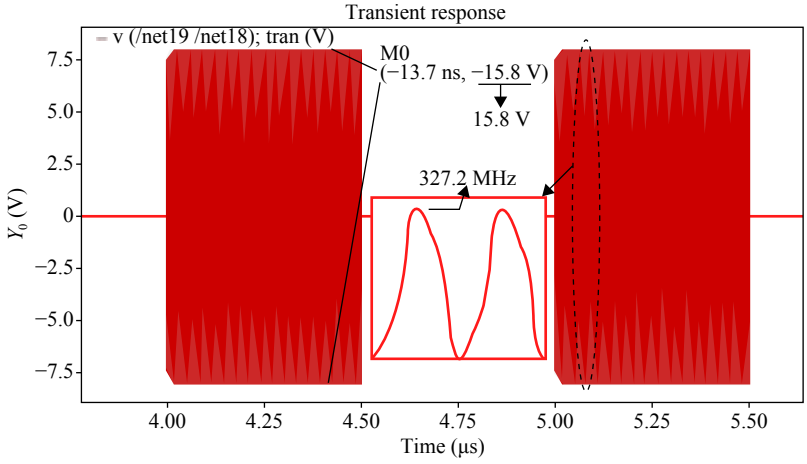

Fig. 5. (Color online) Simulated waveform of the cross-coupled oscillator.

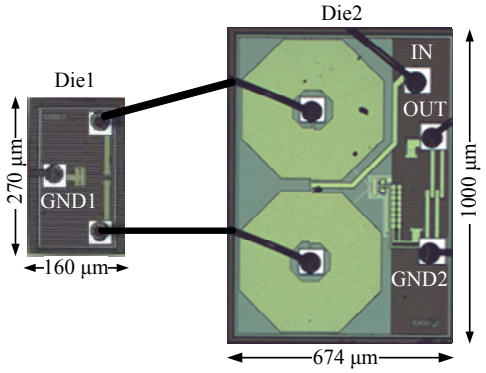

Fig. 6. (Color online) Chip micrograph.

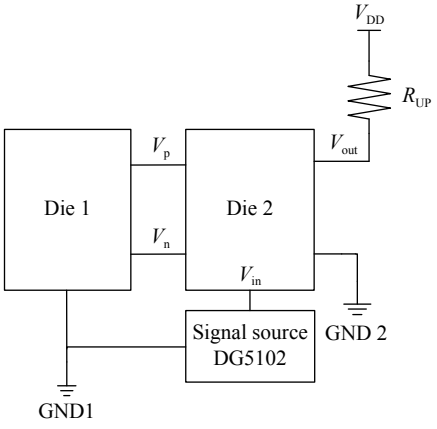

Fig. 7. Measurement setup.

ciple of the full-wave bridge rectifier is that if V_{sp} is positive, MN4 and MP1 are turned on, and if V_{sn} is positive, MN3 and MP2 are turned on. When $V_g > V_T$, MN5 is turned on and the output is connected to ground and V_{out} is set to Low. When $V_g < V_T$, MN5 is turned off and the output is connected to the supply voltage through R_{UP} and V_{out} is set to High. The sizes of rectifier MOS transistors are decided by the output current of the rectifying circuit, which is given by:

$$I_d = \frac{\Delta VC}{\Delta t} = \frac{V_T C_{gg}}{R_{on} C_{gg}} = \frac{V_T}{R_{on}}, \quad (6)$$

where V_T = 800 mV is the threshold voltage of the OD gate

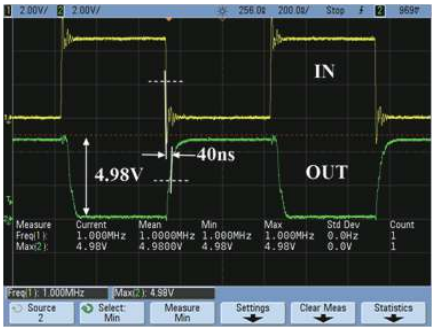

Fig. 8. (Color online) Measured input and output waveforms.

circuit, R_{on} is the on-resistance of the rectifier MOS transistor, and C_{gg} is the gate oxide capacitance of the OD gate circuit. The size of OD gate circuit is designed according to 50 mA drive current. Therefore, the width-to-length ratio of MP1 (MP2), MN3 (MN4), and MN5 are designed as: 20 μm/0.5 μm, 70 μm/0.5 μm, and 40 μm/0.5 μm, respectively.

3. Simulation and measurement results

Fig. 5 shows the simulated waveform of the cross-coupled oscillator. The simulated oscillation amplitude and oscillation frequency are 15.8 V and 327.2 MHz. The simulated oscillating amplitude is greater than the calculated result. For the sake of simplicity, a higher order harmonic of the output voltage is neglected in the calculation.

Fig. 6 shows the packaged chip, which is implemented in a 0.18 μm CMOS process. To measure the performance of the proposed digital isolator, the measurement setup is shown in Fig. 7. The signal is generated by Rigol DG5102.

Fig. 8 shows the measured input and output waveforms at the operating condition (V_{DD} = 5 V @ 1 MHz, R_{up} = 1 kΩ). The chip operates in a supply range from 4.5 to 5.5 V with a maximum propagation delay of 40 ns.

Table 2 summarizes the performance of the proposed digital isolator and compares it to other optocouplers[12, 13]. A 50 mA drive output current is realized. The input current and input power consumption is the smallest, and the signal bandwidth is 1 MHz higher than PC817. While the isolation

Table 2. Performance summary.

Performance	This work	Ref. [12]	Ref. [13]
Input current (mA)	7.1	50	80
Output current (mA)	50	50	50
Signal bandwidth (MHz)	1	0.08	1
Input power consumption (mW)	35.5	70	120
Isolation voltage (kVrms)	0.4	5	5

voltage of this design is only 0.4 kVrms, it can be improved by choosing a thicker isolation layer or other isolation materials with higher breakdown voltage.

4. Conclusion

A 4-port digital isolator based on an on-chip transformer is designed and fabricated in 0.18 μm CMOS process. By testing and certification, the chip has advantages of lower power consumption, higher bandwidth, and smaller volume than other optocouplers. While the isolation voltage of the chip is lower than other optocouplers, there is a lot of room for improvement. The proposed digital isolator can reduce the total system complexity and cost. It is very convenient and economical to replace the common 4-port optocoupler directly in some old designs.

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