Multi-channel Neural Signal Recording System for an Implantable Brain-Computer Interface

Qingya Li[*], Zhiwei Zhang[*†], Mingxia Shi[*] and Xiaoyan Tao[*]

[*]Institute of Automation, Chinese Academy of Sciences, Beijing, 100190, China

[†]CAS Center for Excellence in Brain Science and Intelligence Technology, Shanghai, 200031, China

Email: qingya.li@ia.ac.cn

Abstract—**Simultaneous recordings of neural activity at massive scope, in the long term, and under bio-safety conditions, could provide crucial information, which helps in better understanding the operation mechanism of the brain and promotes the clinical application evolution for the brain-computer interface. For this purpose, a multi-channel neural signal recording system is presented, which can record up to 2048-channel neural signals by multiple connections of a customized collection system. The system consists of a sensor array module, a central controller module, and an upper computer module. Using the modular design method, the sensor array module can be contrived by changing the number of channels. The single-channel data acquisition module has a sampling resolution of 16 bits, and a sampling rate of 30 KSamples/s. The central controller module can establish a connection between the sensor array module and the upper computer module, and control their operations. The upper computer module can display the data results. The system verifies the performance of the multi-channel data acquisition through the analog neural signal.**

I. INTRODUCTION

The brain-computer interface (BCI) for the implantable application is a fascinating technology that allows direct communication between the brain and an external device or computer system. It involves the implantation of electrodes or microchips into the brain, which can detect and decode neural signals to comprehend various neural interactions such as thoughts, cognition, perception, and actions as well as recover neurological diseases such as stroke, Parkinson's disease, Epilepsy, Alzheimer's disease, Schizophrenia, etc. [1-7].

A wide range of researchers take up brain neural recording systems such as Electroencephalogram (EEG), Electrocorticography (ECoG), Magnetoencephalography (MEG), and Functional magnetic resonance imaging (fMRI), but they have insufficient efficiency in the neural signal recording [8-10]. ECoG records only the local field potentials (LFPs) from the cortex surface, disregarding the action potentials (APs or spikes). The LPFs occupy the frequency band of 1-300 Hz with a peak amplitude of approximately 1 mV, whereas the peak amplitude of APs is approximately 100 μV occupying a frequency band of 300 Hz- 5 KHz [11]. An accurate and robust recording of the amplitudes, shapes, and temporal variability of brain signals is very indispensable in neuroscience research.

An efficacious neural signal recording system needs to meet the requirements of high channel count, miniaturized area, system power consumption, and noise performance, so a trade-off between the key requirements is critical in the systematic design, particularly in the implantable scenario. Some literature reported the implanted neuronal signal recording system [12-15], which could acquire the neural signal of small animals such as mice. However, they are still subject to the influence of the channel count, system flexibility, and acquisition range on the signal quality and the recording capabilities, leading to an increase in the risk during the long-term recording period.

Accordingly, in order to better understand the brain functionalities and the operation mechanism of numerous neurons, a multi-channel implantable brain-computer interface system with up to 2048 channels is proposed in the present work. The system is composed of three sub-systems: a Sensor Array Module (SAM) including a 16-sensor unit (SU), a Central Controller Module (CCM), and an Upper Computer Module (UCM). As the system's core, the central controller module manipulates the other two modules to accomplish the task including the acquisition, handling, and transmission of the neural signals. The collected results are displayed on the upper computer with the raw data and processed data in the vitro experiment.

The rest of this article is organized as follows. First, the system configuration of the proposed multi-channel neural signal recording thoroughly is described in Section II. The measurement setup, signal processing flow, the experimental results are represented in Section III. The conclusions are drawn and future work is discussed in Section IV.

II. SYSTEM CONFIGURATION

In this section, the proposed multi-channel neural signal recording system for an implantable brain-computer interface is designed and presented. The details of different components are explored in the following work.

A. System Overview

The developed implantable brain-computer interface system, presented in Fig. 1, is composed of three sub-systems: a Sensor Array Module (SAM) including a 16-sensor unit (SU), a Central Controller Module (CCM), and an Upper Computer Module (UCM). The sensor array module is designed to acquire the brain neural signals, then they are sent to the central controller module, to detect the electrical activity associated with functioning neurons during the various regions of the brain. The central control module manipulates the operation process of the multiple sensor units and obtains the sampling results in parallel through the interface. The upper computer module can establish communication with the central controller module through the Universal Serial Bus (USB) port. The three sub-systems collaborate closely to complete the recording of electrophysiological activity of the brain cells.
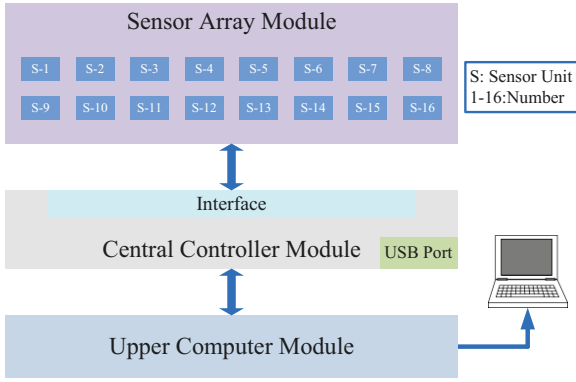
Fig. 1. System architecture.

B. Sensor Array Module

The sensor array module is comprised of 16 sensor units, each sensor unit concludes two commercial integrated chips of RHD2164, two MOLEX connectors with 64-pin, and an FPC interface, as shown in Fig. 2. There are three main functions: (1) Detect and amplify the weak bioelectricity signals of brain, and deliver them to the analog-to-digital converter (ADC); (2) Convert the amplified analog signals into the digital signals with ADC, and buffer the sampled results; (3) Receive and implement the signaling received from the upper computer module.
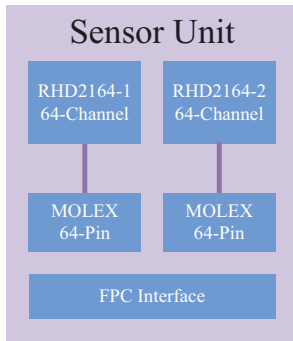

Fig. 2. The architecture of one sensor unit.

Fig. 3 depicts the simplified diagram of RHD2164, which consists of the analog amplifier, analog multiplexer, 16-bit ADC, and standard four-wire 16-bit SPI interface. Each RHD2164 has a 64-channel to identify the neural signals, which is controlled via a 16-bit SPI bus with a 24 MHz clock frequency. The analog amplifier operates as a normal amplifier to magnify the weak neural signals from the 64 channels. The analog multiplexer (MUX) is used to choose the needed channel within all 64 channels and allows many amplifiers to share the on-chip ADC. The ADC can sample each channel up to 30 kSamples/s. The SPI interface is composed of four signals: an active-low chip select ($\overline{CS}$), a serial data clock (SCLK) with a base value of zero, a "Master Out, Slave In" data line (MOSI) to receive commands from the master devices, and a "Master In, Slave Out" data line (MISO) to send pipelined results from prior commands to the master device.
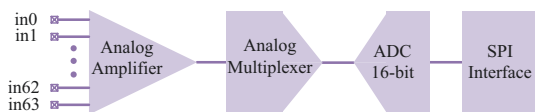

Fig. 3. The simplified diagram of RHD2164.

Inspection of Fig. 4 shows the connection diagram between the FPC interface and two RHD2164 chip 1 and chip 2 through the SPI interface protocol. RHD2164 chip 1 and chip 2 share a common SCLK and MOSI, whereas $\overline{CS}$ and MISO are independent of each other.
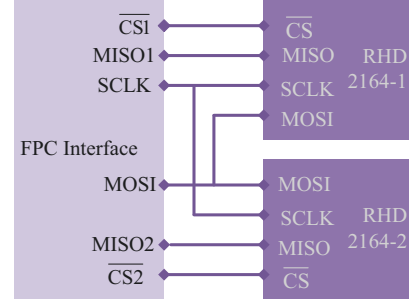

Fig. 4. The connection diagram between the FPC interface and two RHD2164 chips.

C. Central Controller Module

The main significant function of the central controller module is to accomplish the data interaction with the upper computer module through USB protocol, forward the signaling received from the upper computer to the sensor array module, and upload the sampling results of the sensor array module to the host computer. The hardware structure of the central controller module is shown in Fig. 5.
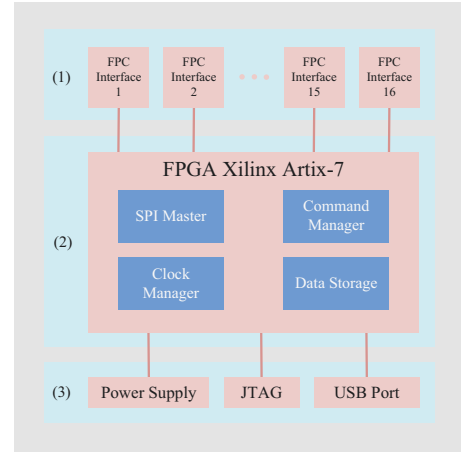

Fig. 5. The hardware structure of the central controller module.

The central controller module is divided into three portions: (1) sixteen FPC interfaces, connecting the central controller module and sensor array module; (2) an FPGA Xilinx Artix-7, dominating the control functions; (3) three auxiliary units, including power supply, JTAG, and USP port, which can offer the power for the whole system, transfer the debug information, and communication with the upper computer, respectively.

The FPGA, as the significant function implementer of the central controller module, can provide commands and data handling functionality to the other modules. It is split into four parts: an SPI master, a command manager, a clock manager, and data storage. The SPI master provides a full-duplex interface for commanding the bio-signal front-end and receiving digitized samples. The command manager furnishes control instructions for the entire system, including data processing, data storage, data transmission, instruction code transmission, instruction execution, and so on. The

clock manager produces the operating needed clocks of the system. The data storage could save the experimental results.

D. Upper Computer Module

The upper computer module can receive the acquisition results from the sensor array through the USB cable, and display them on the computer window. As shown in Fig. 6, the upper computer module is composed of two parts: (1) Settings, including sampling rate, time duration, channel selection, and storage settings; (2) Graphical User Interface (GUI), encompassing (2-1) Raw Data Waveform window and (2-2) Spike Signal Waveform window, which could present the original recording neural signal and spike signal waveforms in real-time. The simultaneous viewable number of channels in the (2-1) and (2-2) window is 128 on the computer screen, respectively.
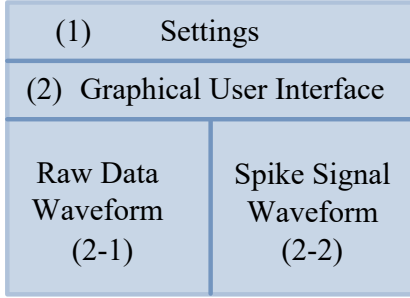
(1) Settings	
(2) Graphical User Interface	
Raw Data Waveform (2-1)	Spike Signal Waveform (2-2)

Fig. 6. The structure of the upper computer module.

III. RESULTS AND DISCUSSION

To better verify the basic performance of the developed multi-channel neural signal recording system, a series of experiments are conducted and the results are drawn out in the following work.

A. Experimental Setup

In this work, an experimental testing platform of a multi-channel neural signal acquisition system is established, as shown in Fig. 7 (a) and Fig. 7 (b). The signal generator offers the input signal for the sensors, which could be expressed by a sinusoidal wave signal produced by the waveform generator, the neural signals generated by the neural signal simulator, or neural signals gathered by the animal experiments. There are 16 sensors to acquire the signal. When the sensors accept the input signals, then the collected results will be transmitted to the FPGA. Finally, the recording data results would be delivered to the upper computer utilizing the USB cable. In this way, the signal collection process is accomplished.
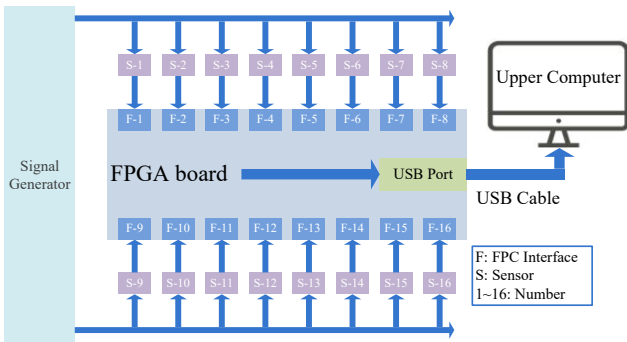
(a) The block schematic diagram of the testing system
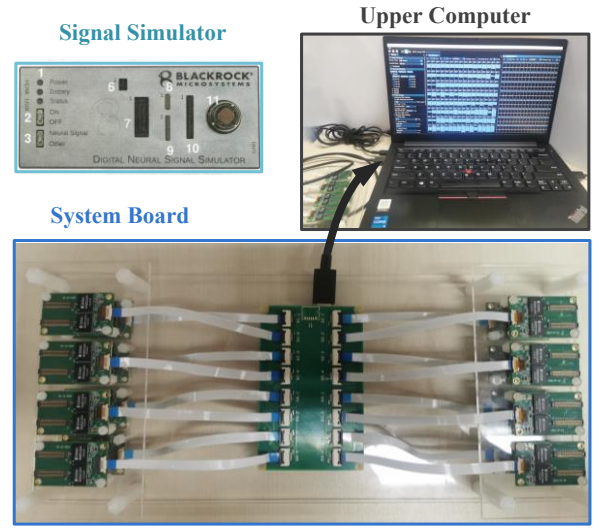
(b) The image of testing system

Fig. 7. The testing platform of the multi-channel neural signal acquisition system.

B. The Working Flowchart

To achieve the function validation of the proposed multi-channel neural signal recording system, including data acquisition, sending and receiving signaling results, and corresponding control commands, a working flowchart is designed, as shown in Fig. 8. The primary responsibilities include: (1) Initialize the interface and memory; (2) Establish a communication link between the three sub-systems; (3) Transmit, receive, and parse the related instructions, and execute the corresponding actions.
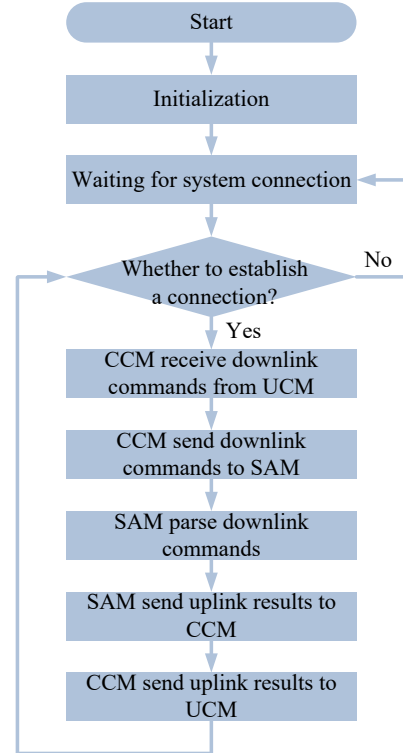

Fig. 8. The working flowchart of the proposed system.

C. Experimental Results

To achieve the functional verification of the proposed multi-channel neural signal recording system, a series of

experiments are conducted and experimental results and analysis are given in the following work.

(1) The protocol format of recording signals

The entire neural signal recording system contains 2048 channels, a dedicated signaling protocol is designed for the data upload, and the protocol format of a data packet is shown in Table I. The data packet contains the sampling results of 64 channels, including a 32-bit header and 32-bit data, as shown in TABLE I. The header is composed of a 16-bit magic number (BBAA), an 8-bit sequence number, a 4-bit group number ranging from 0-3, and a 4-bit channel number ranging from 0-7. The data is divided into two sections: low 16-bit and high 16-bit, which could indicate the acquisition results of channel A and channel B, respectively. The measured results are shown in Fig. 9. The data in the dashed box display the header. The test results are displayed between the two dashed boxes, which are FFFF due to the no connection of the sensor array module.

TABLE I. PROTOCOL FORMAT OF THE SAMPLING DATA PACKAGE

Header	Values		Bits
Magic number	BBAA	Constant	16
Sequence Number	0-255	cycle counter	8
Group Number	0-3	00,01,10,11	4
Channel Number	0-7	0000000,1111111(0-127)	4
Data	Values		Bits
Low 16 bits	Results of channel A		16
High 16 bits	Results of channel b		16

Fig. 9. The measured results about the header.

When the data acquisition process has been finished, there is an ending flag of the results using the 32-bit DDCCBBAA, as shown in TABLE II. Fig. 10 presents the experimental results with the ending flay of DDBBCCAA at the dashed box.

TABLE II. ENDING FLAG OF THE SAMPLING

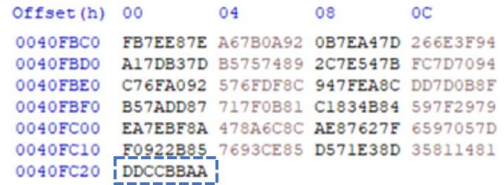| Data	Meaning	Bits
DDCCBBAA	The ending flag of sampling	32

Fig. 10. The measured results about the ending flag.

(2) The performance test of the proposed system

The system performance test adopts the neural signal simulator, which is capable of simulating two distinct for testing purposes. One is the neural signal including the spike signal and LFP signal, and the other is sine sweep with the mixed sine signal. Accordingly, three different situations of the input signal are conducted in the work, as shown in Fig. 11 -Fig. 13.

In the measurement process, the output signal waveforms are consistent for all the channels of the neural signal simulator, which makes the input and output signals for the proposed system consistent. Therefore, the sampling results of one channel, as the representative example, are selected to validate the system, as shown in Fig. 11-Fig. 13. These results demonstrate the designed multi-channel system performs fine behavior of the neural signal capture and spike signal detection.
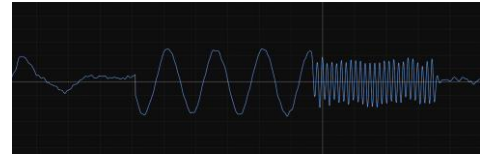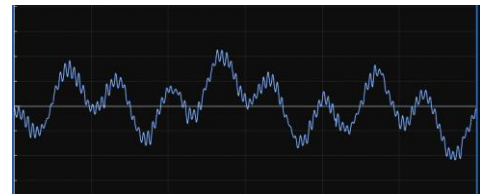

Fig. 11. The mixed sine signal results.
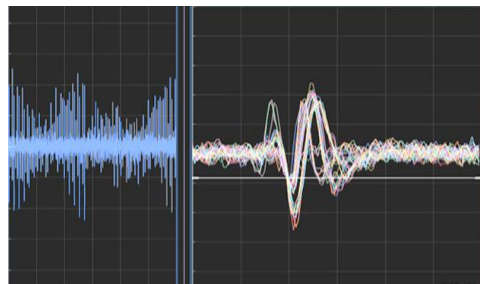

Fig. 12. The LFP signal results.

Fig. 13. Both of raw signal and spike signal results

IV. CONCLUSION

In this work, a multi-channel synchronous neural signal recording system has been explored elaborately for the implantable brain-computer interface applications. The proposed system contains three elements: a Sensor Array Module, a Central Controller Module (CCM), and an Upper Computer Module (UCM), whose structures are introduced in detail. The sensor array module can be flexibly combined

by adopting the modular design. The central controller module establishes communication with the upper computer module through the USB cable and controls the operation process of the sensor array module employing sampling protocol. The system verifies the applicability successfully to collect the analog mixed sine signals and neural signals including the LFP and spike signals in the vitro experiment. The future work will pay more attention to the vivo experiment in rats or non-human primates using actual implantation, and demonstrate the accuracy and feasibility of the designed system.

REFERENCES

[1] V. Chandrasekhar, V. Vazhayil, and M. Rao, "Design of a real time portable low-cost multi-channel surface electromyography system to aid neuromuscular disorder and post stroke rehabilitation patients," Proc. 42nd Annu. Int. Conf. IEEE Eng. Med. Biol. Soc. (EMBC), Jul. 2020, pp. 4138–4142.

[2] M. Gharaei Jomehei and S. Sheikhaei, "A low-power low-noise CMOS bio-potential amplifier for multi-channel neural recording with active DC rejection and current sharing," Microelectron. J., vol. 83, pp. 197–211, Jan. 2019.

[3] A. Zabihian and A. M. Sodagar, "A new architecture for multi-channel neural recording microsystems based on delta-sigma modulation," Proc. IEEE Biomed. Circuits Syst. Conf., Nov. 2009, pp. 81–84.

[4] R. Ranjandish and A. Schmid, "A review of microelectronic systems and circuit techniques for electrical neural recording aimed at closed-loop epilepsy control," Sensors, vol. 20, no. 19, p. 5716, Oct. 2020.

[5] W.-C. Chen, C. W. L. Lee, A. Kiourti, and J. L. Volakis, "A multichannel passive brain implant for wireless neuropotential monitoring," IEEE J. Electromagn., RF Microw. Med. Biol., vol. 2, no. 4, pp. 262–269, Dec. 2018.

[6] M. Komatsu, K. Takaura, and N. Fujii, "Mismatch negativity in common marmosets: Whole-cortical recordings with multi-channel electrocorticograms," Sci. Rep., vol. 5, no. 1, pp. 1–7, Oct. 2015.

[7] M. A. Bin Altaf, C. Zhang, and J. Yoo, "A 16-channel patient-specific seizure onset and termination detection SoC with impedance-adaptive transcranial electrical stimulator," IEEE J. Solid-State Circuits, vol. 50, no. 11, pp. 2728–2740, Nov. 2015.

[8] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 804–816, Apr. 2010.

[9] K. Abdelhalim, L. Kokarovtseva, J. L. P. Velazquez, and R. Genov, "915-MHz FSK/OOK wireless neural recording SoC with 64 mixed-signal FIR filters," IEEE J. Solid-State Circuits, vol. 48, no. 10, pp. 2478–2493, Oct. 2013.

[10] S. Brenna, F. Padovan, A. Neviani, A. Bevilacqua, A. Bonfanti, and A. L. Lacaita, "A 64-channel 965-μW neural recording SoC with UWB wireless transmission in 130-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 6, pp. 528–532, Jun. 2016.

[11] B. Ji, Z. Liang, X. Yuan, H. Xu, M. Wang, E. Yin, Z. Guo, L. Wang, Y. Zhou, H. Feng, et al., "Recent advances in wireless epicortical and intracortical neuronal recording systems," Science China Information Sciences, vol. 65, no. 4, p. 140401, Apr. 2022.

[12] K. Keramatzadeh, A. Kiakojouri, M. S. Nahvi, Y. Khazaei, A. Feizi-nejad, M. H. Maghami, R. Mohammadi, M. Sharifshazileh, S. Nasiri, F. Akbari Boroumand, et al., "Wireless, miniaturized, semi-implantable electrocorticography microsystem validated in vivo," Scientific Reports, vol. 10, no. 1, p. 21261, Dec. 2020.

[13] A. Zhou, S. R. Santacruz, B. C. Johnson, G. Alexandrov, A. Moin, F. L. Burghardt, J. M. Rabaey, J. M. Carmena, and R. Muller, "A wireless and artefact-free 128-channel neuromodulation device for closed-loop stimulation and recording in non-human primates," Nature Biomedical Engineering, vol. 3, no. 1, pp. 15–26, Jan. 2019.

[14] S. Idogawa, K. Yamashita, R. Sanda, R. Numano, K. Koida, and T. Kawano, "A lightweight, wireless Bluetooth-low-energy neuronal recording system for mice," Sensors and Actuators B: Chemical, vol. 331, p. 129423, Mar. 2021.

[15] S. Luan, I. Williams, M. Maslik, Y. Liu, F. De Carvalho, A. Jackson, R. Q. Quiroga, and T. G. Constandinou, "Compact standalone platform for neural recording with real-time spike sorting and data logging," Journal of Neural Engineering, vol. 15, no. 4, p. 046014, Aug. 2018.