Including the Effects of Process-Related Variability on Radiation Response Using a New Test Chip

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Abstract

Space applications using advanced foundry processes require accurate assessment of the dependence of total-ionizing dose (TID) response on process variability and layout. A new test chip is described to enable large sample of device measurements under irradiation. The variability of TID-induced leakage current and transistor mismatch both increase after irradiation.
Keyword: Radiation effects, TID, Mismatch, Stress, Process Design Kit, Process Variability.

1. Introduction

As CMOS technology aggressively scales down, device variability (due to process variations and layout dependent effects caused by factors like strain) becomes a major issue. Accurate assessment of effects such as transistor mismatch is not only required by commercial designs using advanced processes, but also required by space applications, since previous work has shown that total ionizing dose (TID) response is sensitive to process variations and layout [1]-[4]. Many space applications rely on commercial foundries to provide advanced process technologies, but how to enhance foundry process design kits (PDKs) accurately and quickly to address the space environment is another challenge. Getting statistically significant on-wafer measurements of radiation response is often difficult, as radiation tests require the devices under test to be biased, and unless special precautions are taken, radiation will damage all the devices on the same die. Also, one has to measure quickly to avoid annealing. This paper presents a new characterization approach to address TID effects. The approach is verified with 90 nm and 65 nm processes.

2. Test Chip

The test circuit used in this work consists of a 64X4 transistor array, with a capacity of 256 transistors per array. The array was originally designed for transistor mismatch characterization [5], and for characterizing the process variability of TID response. We modified the array to include the following elements: (1) identical transistors to get statistical measurements; (2) transistors of different geometries from which pre-irradiation and post-irradiation SPICE models can be extracted; and (3) transistors with different layout variations that affect the STI stress. This allows the investigation of layout effects on TID response. The array is designed to maintain the same local environment for different devices to preserve uniformity, and the routing is also designed carefully to avoid asymmetry. The organization of the array is shown in Fig. 1, which allows the devices to be biased during irradiation and measured quickly. Gate controls (rows) are multiplexed using a 64X shift-register, and each array column is directly connected to an external pad, avoiding the need for more complex decoding circuitry.

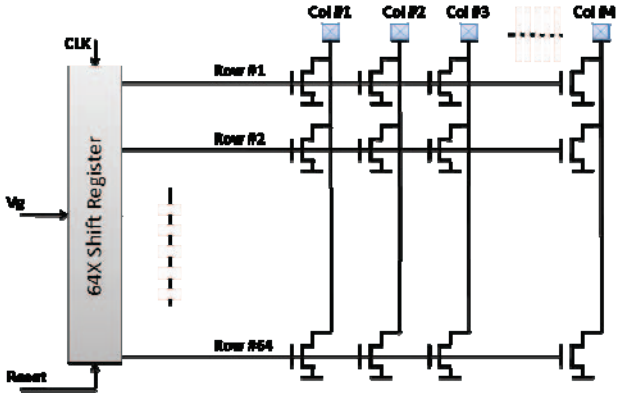

Fig. 1. Transistor array schematic circuit diagram.

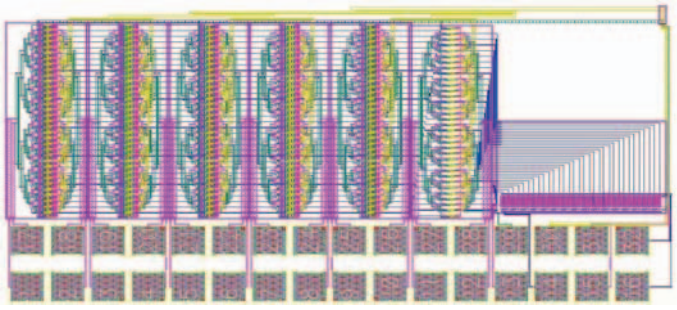

Fig. 2. Transistor array layout.

Since we primarily are investigating the increased

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leakage due to TID-induced degradation of the STI, the following techniques were used: (1) each column contains devices with the same geometry and layout; (2) the current was measured with all gates turned off on the same column to determine the total leakage reference or "floor" current; and (3) the individual drain current of each device in a column was measured by sending the appropriate control gate signal and subtracting the "floor" current. The chip layout is shown in Fig. 2. The test vehicle is laid out with a 2X16 pad frame containing six arrays, which allows the testing of 1536 transistors with a single probing operation. The test chip was fabricated in 90-nm and 65-nm CMOS technologies.

3. Experimental Results

One difficulty in obtaining accurate estimates of TID response is that the individual device response may be highly variable. Because of process variations, one needs device-level statistical measurements to produce accurate estimates of circuit-level degradation. Fig. 3 compares the off-state leakage current (measured at drain voltage Vd = 1.2 V and gate voltage Vg = 0 V) at a total dose of 100 krad(SiO2) of a standard threshold voltage *Vt* device (AVT) to that of a high *Vt* device (HVT) and low *Vt* device (LVT). These correspond to three different process options. Samples from three different die in the 65-nm process are included to illustrate the level of variability. Each die location leads to a different conclusion about the relative radiation susceptibility of the different process variants, demonstrating the need to use statistically based measurements to prevent measurement instability and better calibrate models in chip-level design. Using the test chip, we evaluated the TID response of the different process variations. Fig. 4 shows typical results selected from a large sample of device measurements. Overall, the HVT devices are less sensitive to TID compared to the LVT devices.

Statistical analysis was performed to investigate the leakage distribution before and after irradiation. Fig. 5 displays the histogram plots of transistor leakage current before and after irradiation. The standard deviation of the off state leakage current at 100 krad(SiO2) increases slightly compared to that of the pre-irradiation off state leakage current. The standard deviation of the leakage current measured at 300 krad(SiO2) shows a more obvious increase compared to that measured at 100 krad(SiO2). Besides the inherent process variations such as variations of oxide thickness, doping concentration and transistor length or width, etc., the non-uniformity of trapped charge and the interface traps induced by irradiation may add more variability, increasing the standard deviation of the device parameters as the dose increases up to certain total dose. This trend is seen in the experimental data.

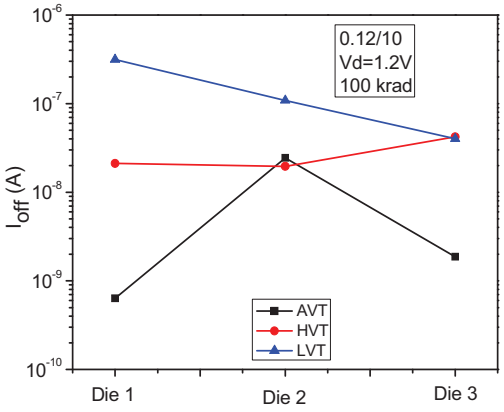
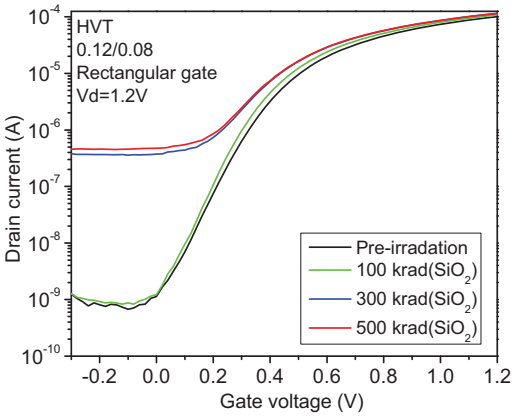
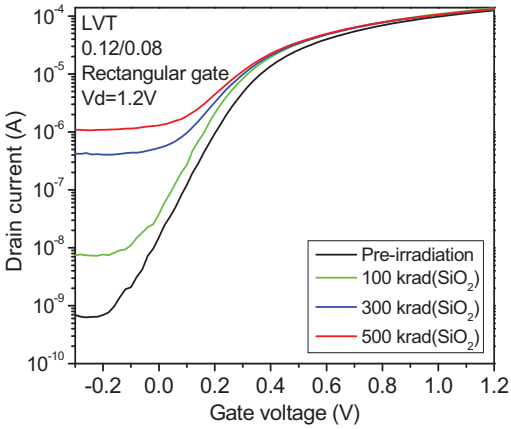


Fig. 3. Post-irradiation I_{off} of different process variants from three different die.



(a)



(b)

Fig. 4. I_d-V_g curves before and after irradiation for (a) HVT and (b) LVT devices.

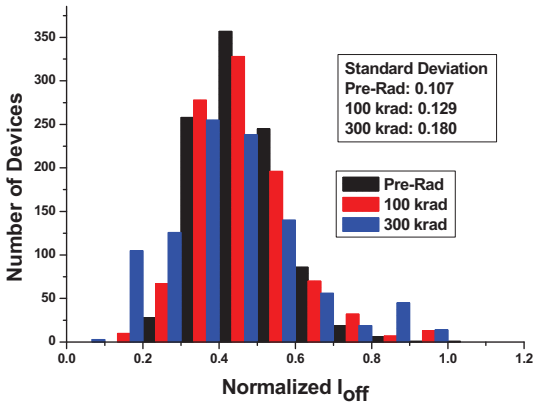


Fig. 5. Histogram plot of leakage current for a NMOS transistor with W=0.12 µm, L=0.08 µm.

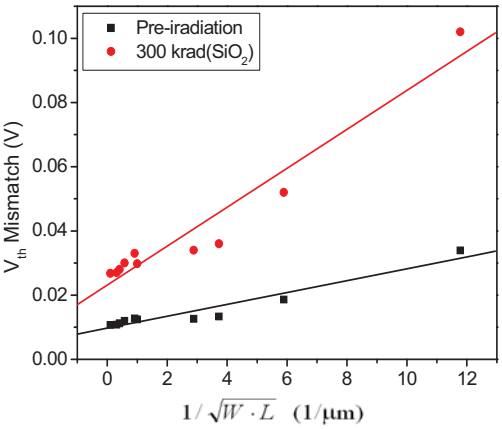


Fig. 6. Pelgrom plot of linear V_t mismatch for NMOS transistors.

Linear V_t mismatch measurements were also carried out with the array, with the sample of 256 transistors providing good statistics. Fig. 6 shows the Pelgrom plot [6] of linear V_t mismatch results obtained before irradiation and after a total dose of 300 krad(SiO_2). The V_t mismatch increases significantly after irradiation, with the average ΔV_t increasing by almost 3X, and some devices showing over 100 mV of ΔV_t with V_t = 0.35 V. This greatly limits the performance of high precision analog circuits in space environments [7] and requires special care during circuit design to mitigate the damage. The increase of V_t mismatch proves again that TID induces more local variability to device performance.

The test chip also enabled us to investigate TID response dependence on other process variations, including variation that affects the STI stress. Fig. 7 shows the post-irradiation leakage current variation with active-to-active distance, showing that the TID-induced leakage current increases with increasing active-to-active distance. The TID-induced current depends on this layout variable due to changes in the doping profile under different STI stresses, since the dopant diffusion coefficient is stress dependent [8].

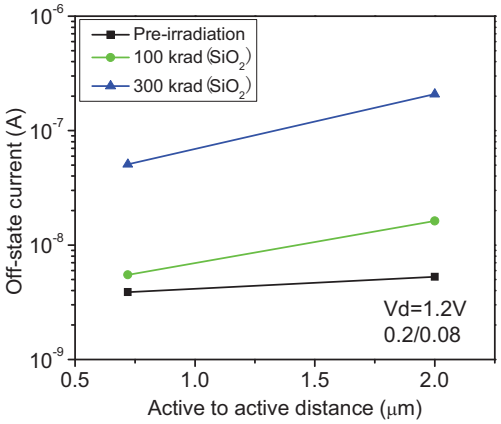


Fig. 7. Pre- and post-irradiation off-state current evolution with active to active distance.

4. Summary

A new characterization approach for addressing the effects of process-related variability on TID response is described. The approach is demonstrated using a new test chip that includes transistor and circuit-level elements. Experimental results show that the variability of TID-induced leakage current and transistor mismatch both increase after irradiation.

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